

87654321

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REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
A	INITIAL RELEASE	07SEP23	M. CEE
A	CHANGES PER ECR-124234	10JAN25	M. CEE

EVAL-AD9954-ARDZ SCHEMATIC REV (A)

PAGE 2 - POWER CIRCUIT & ARDUINO HEADER

PAGE 3 - AD9954 CIRCUIT

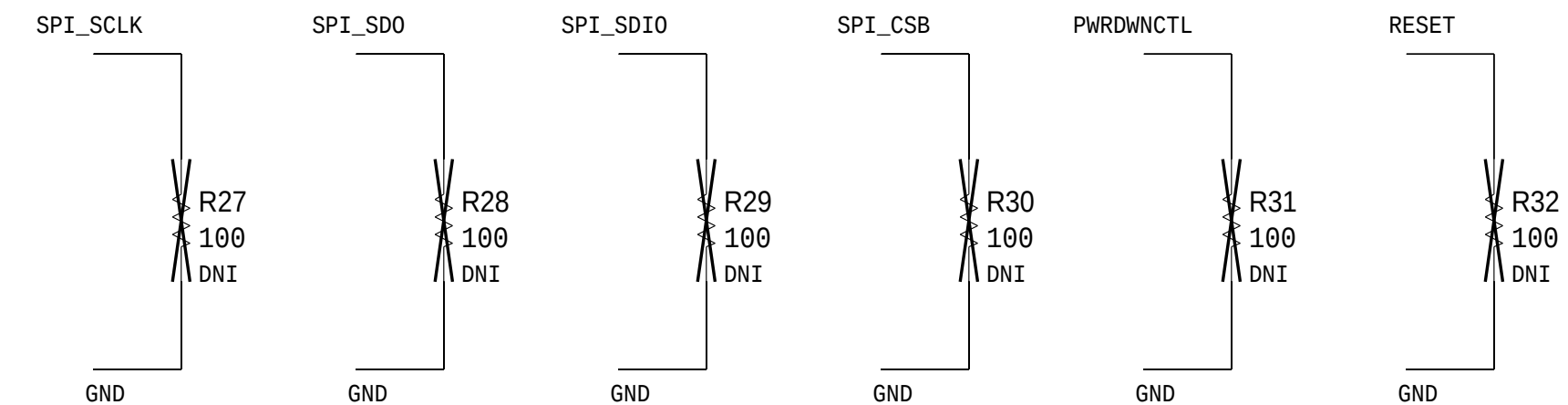
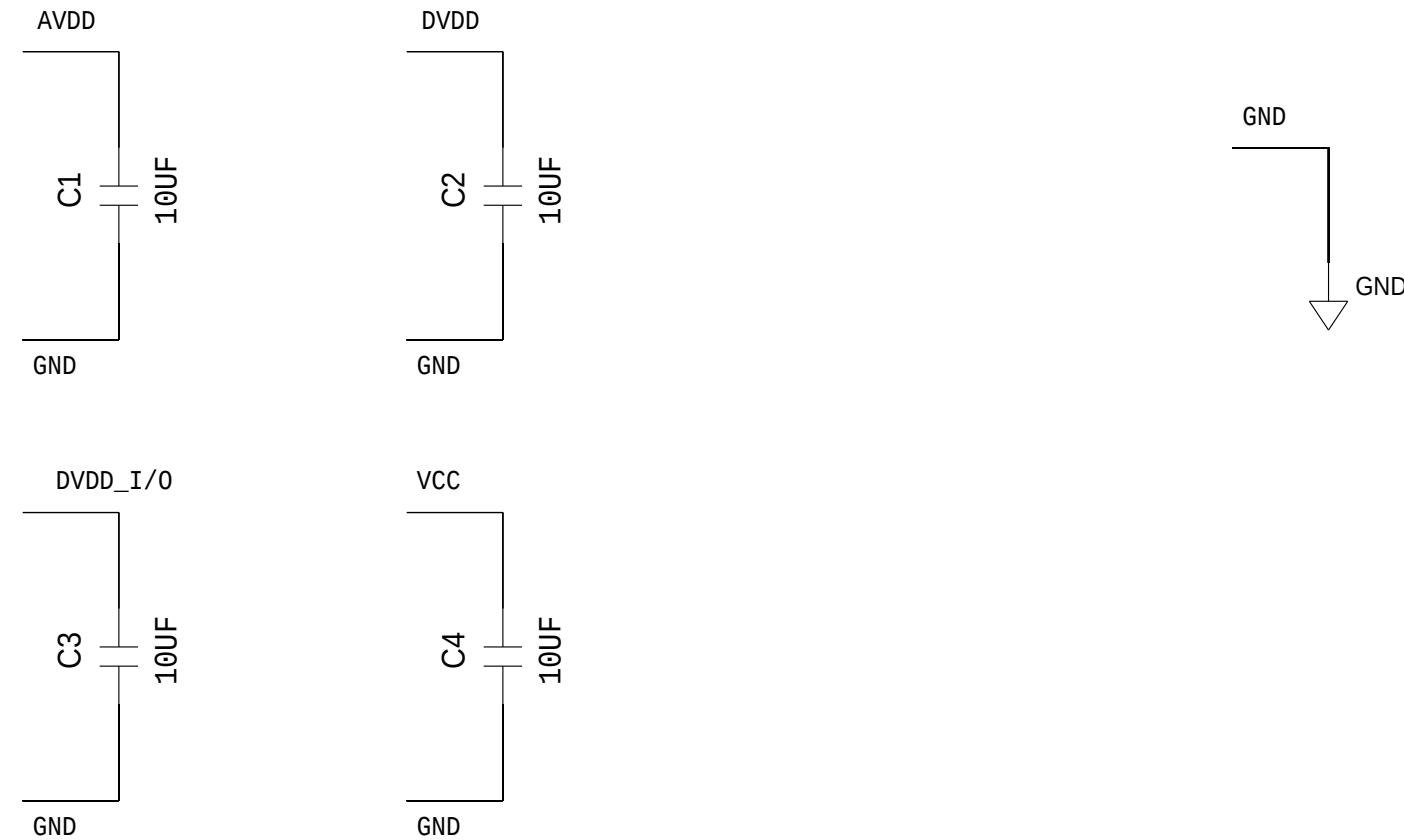
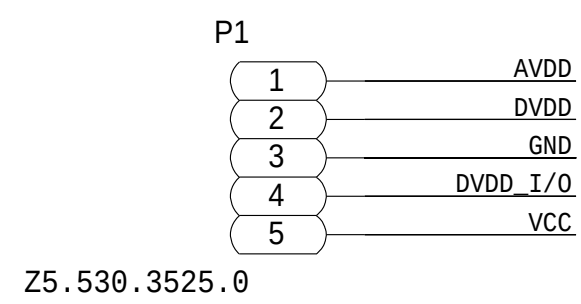
P.O SPEC.	BK/BD SPEC.	SOCKET OEM	OEM PART#	HANDLER

TEMPLATE ENGINEER -	DATE	SCHEMATIC					
HARDWARE SERVICES M. VALE	07SEP23						
HARDWARE SYSTEMS -		HW TYPE : Customer Evaluation Z Product(s): AD9954 : AD9953, AD9952, AD9951, AD9859 PACKAGE : LeadCount-lead 7X7_MM TQFP_EP-family : Pitch-pitch StyleVendor Style <User Define> <User Define> <User Define>					
TEST ENGINEER -							
COMPONENT ENGINEER N. CATALAN	07SEP23						
TEST PROCESS -							
HARDWARE RELEASE K. JABATAN	07SEP23						
DESIGNER E. DELOS REYES	07SEP23	MASTER PROJECT TEMPLATE TBD	TESTER TEMPLATE 064489_c	DRAWING NO. 02_076302-02	REV. B		
PTD ENGINEER M. CEE	07SEP23	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES DECIMALS X.XX +-0.010 FRACTIONS +-1/32 ANGLES +-2					
CHECKER -				SIZE D	SCALE 1:1	CODE ID NO. CodeID	SHEET 1 OF 3

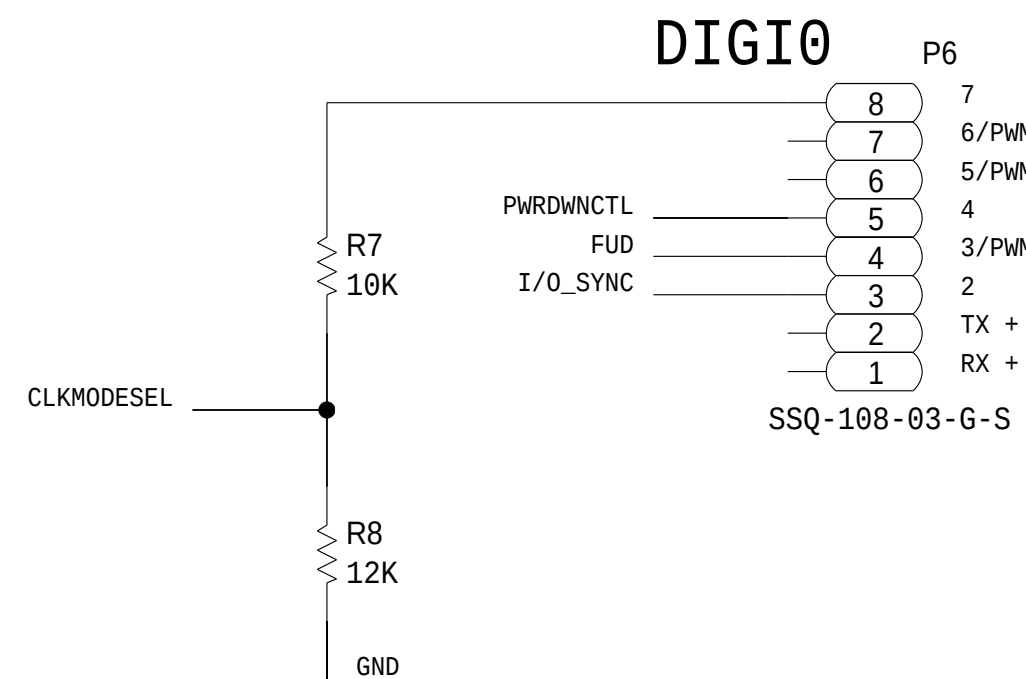
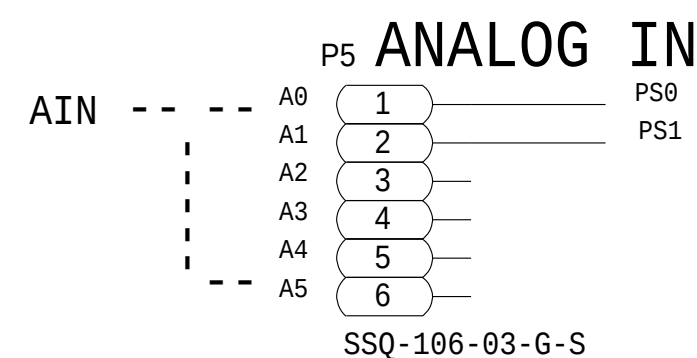
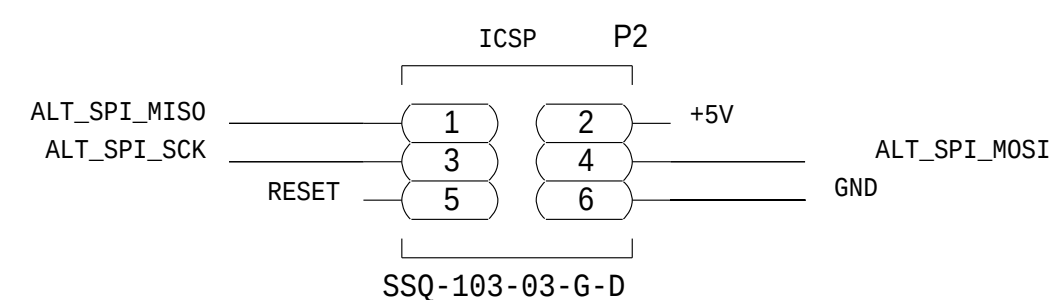
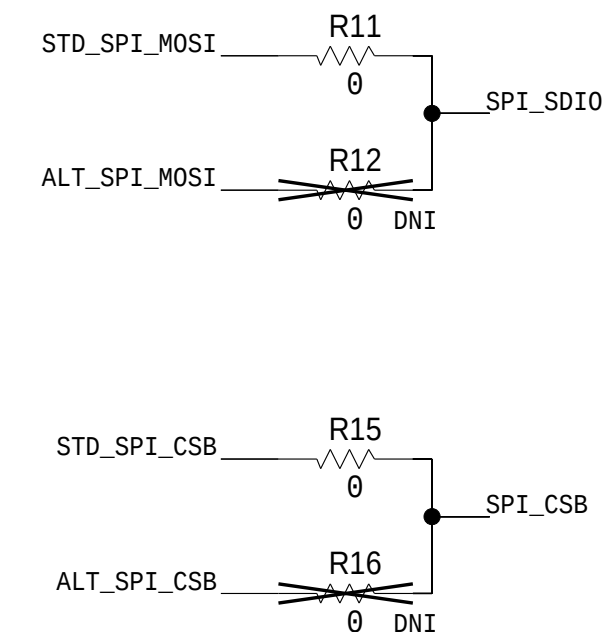
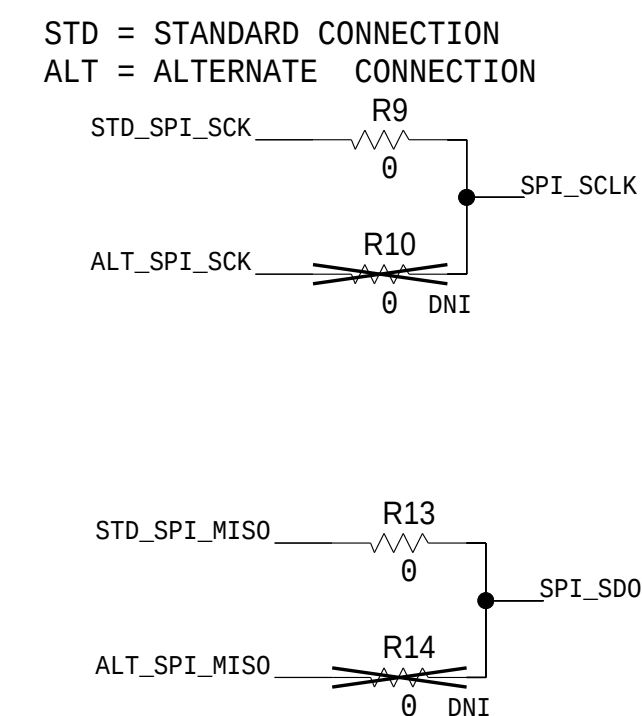
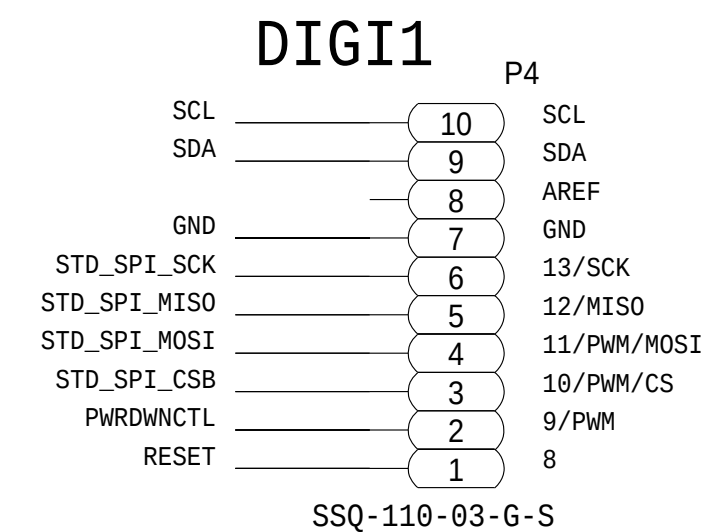
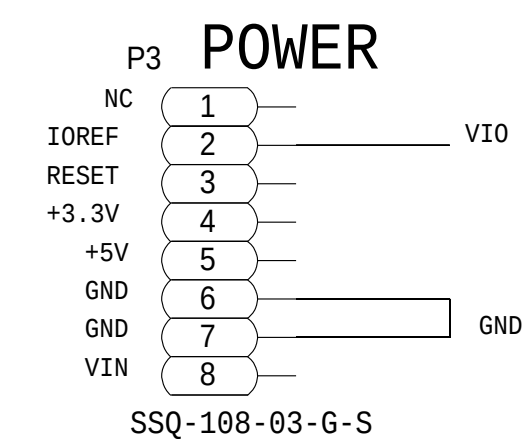
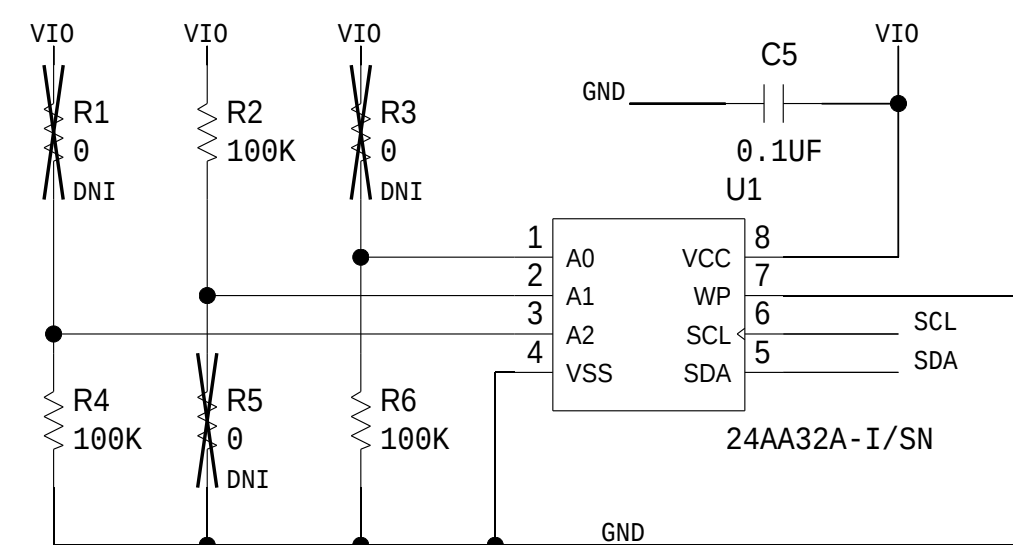
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POWER CIRCUIT

PULLDOWN RESISTORS



ARDUINO UNO SHIELD TEMPLATE (REV B)



NOTE: USING THE UART SIGNALS MAY INTERFERE WITH THE SERIAL MONITOR ON OFFICAL ARDUINO BOARDS SUCH AS THE UNO, MEGA, DUE, ETC.

SCHEMATIC					
HW TYPE : Customer Evaluation Z					
Product(s): AD9954					
: AD9953, AD9952, AD9951, AD9859					
DESIGN VIEW <DESIGN_VIEW>			DRAWING NO. 02_076302-02		REV B
PTD ENGINEER M. CEE			SIZE D	SCALE 1:1	SHEET 2 OF 3

NOTE 1

THE FULL-SCALE DAC OUTPUT CURRENT IS CONTROLLED BY MEANS OF AN EXTERNAL RESISTANCE R25 (RSET) CONNECTED BETWEEN THE DAC RSET PIN AND GROUND. RESISTOR VALUES FOR FULL-SCALE CURRENT ARE AS FOLLOWS: 3.92KOHM = 10MA, 5.23KOHM = 7.5MA, 7.87KOHM = 5.0MA, 15.8KOHM = 2.5MA

NOTE 2

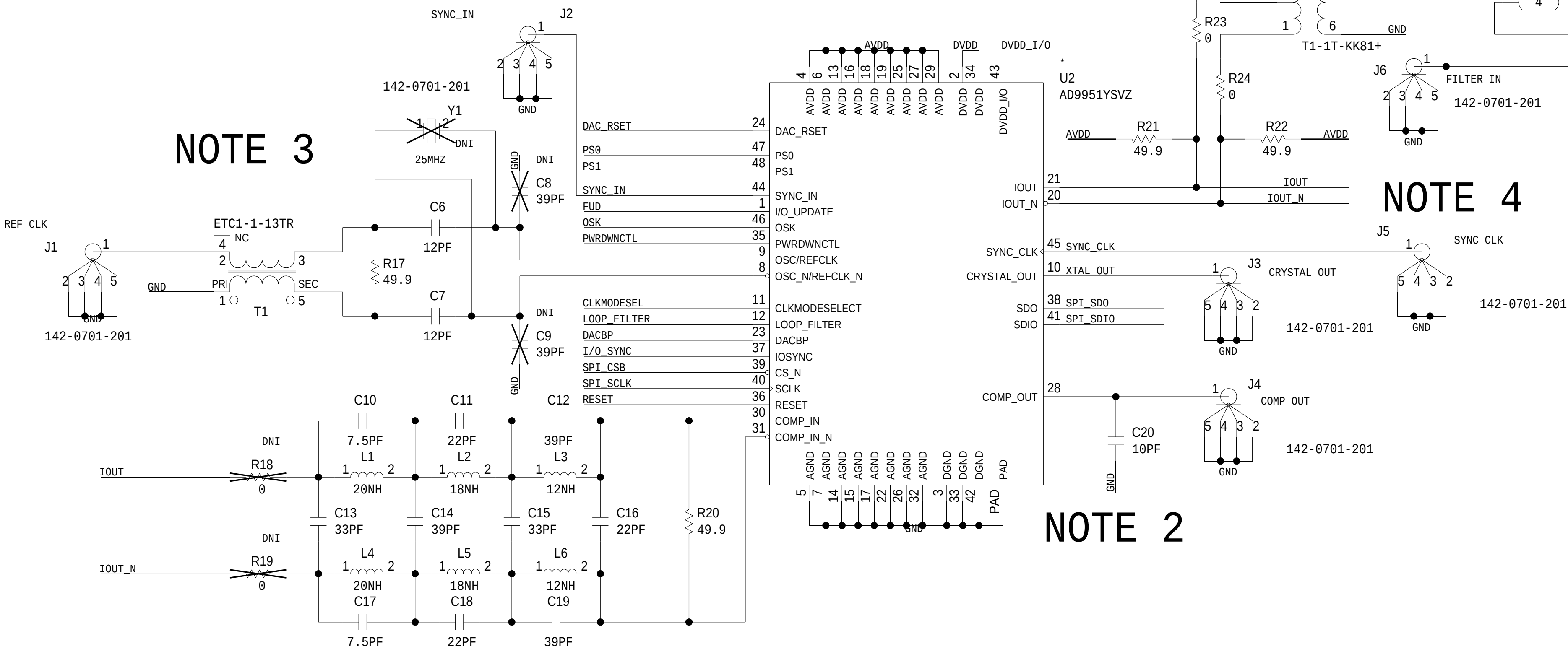
C20 IS USED FOR A SIMULATED CAPACITANCE LOAD FOR THE COMPARATOR OUT. THIS CAPACITANCE VALUE SHOULD NOT EXCEED 10PF.

NOTE 3

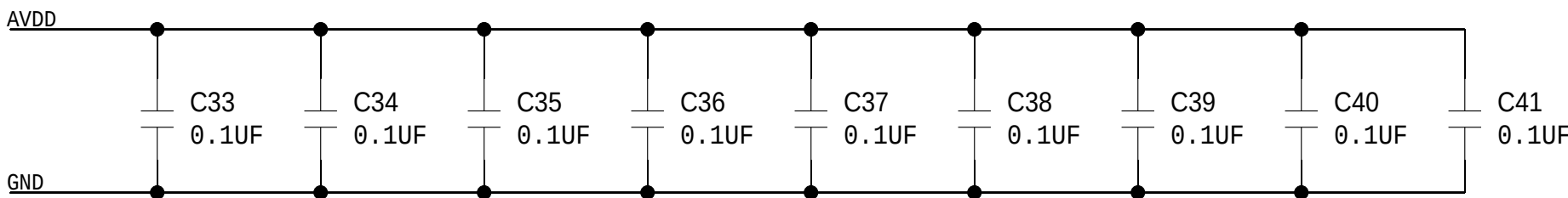
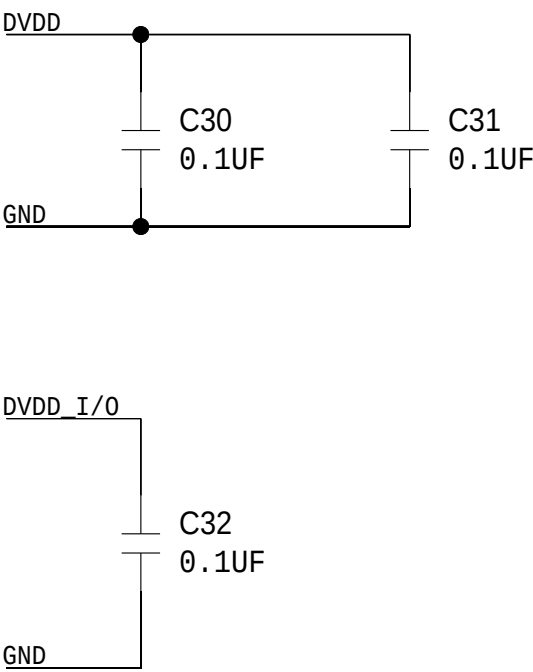
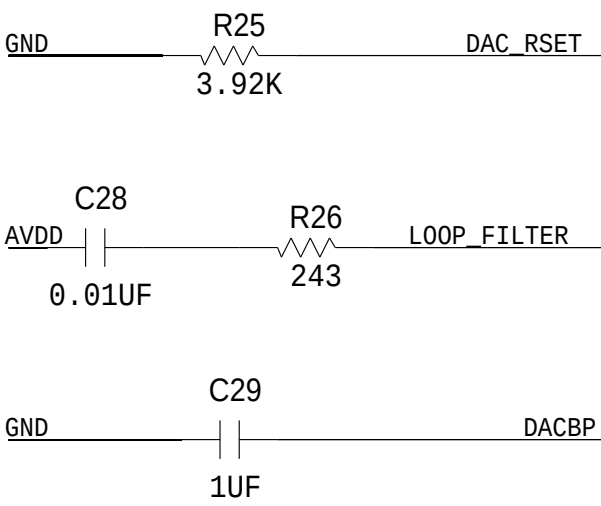
CAPACITORS C6 AND C7 SHOULD BE SOLDERED IN PLACE WHEN THE REF CLK INPUT IS USED. CAPACITORS C8 AND C9 SHOULD BE SOLDERED IN PLACE WHEN CRYSTAL Y1 IS USED IN CONJUNCTION WITH THE INTERNAL OSCILLATOR.

NOTE 4

USE EITHER RESISTORS R18 AND R19 (COMPARATOR INPUTS) OR R23 AND R24 (FILTERED OUTPUT) FOR IOUT AND IOUTB. DO NOT USE BOTH SETS AT THE SAME TIME.



NOTE 1



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DESIGN VIEW <DESIGN_VIEW>			DRAWING NO. 02_076302-02		REV B
PTD ENGINEER M. CEE			SIZE D	SCALE 1:1	SHEET 3 OF 3